AMENDMENTS TO THE DRAWINGS:

Figures 1-3 have been amended to remove the "3/3" numbering from the top of Figure 1, the "2/3" numbering from the top of Figure 2, and "1/3" numbering from the top of Figure 3.

REMARKS

The application has been amended and is believed to be in condition for allowance.

Objections to the Specification

The Official Action states that the title of the invention is not descriptive, and that a new title is required that is clearly indicative of the invention to which the claims are directed.

In response, the title has been amended responsive to the Official Action's objection.

The Official Action objects to the disclosure due to informalities on pages 1, 4, and 5 of the specification.

The specification has been responsively amended to obviate the objection.

Objections to the Drawings

Figures 1-3 have been amended to remove the "3/3, "2/3", and "1/3" numbering from the top of Figure 1, Figure 2, and Figure 3, respectively.

Objections to the Claims

The Official Action objects to informalities cited on claims 1 and 8.

The claims have been responsively amended.

Formal Rejections: 35 USC 112, second paragraph

The Official Action rejects claims 2-4, 6, 9-11, and 13 under 35 USC 112, second paragraph, as indefinite for failing to particularly point out and distinctly claim the subject matter which applicants regard as the invention.

As to claims 2 and 9, the Official Action states that the phrasing "the interface engine is adapted to sent the device control code to the external device, or the request output is based at least partly on the device control code" is unclear. Claims 3-4 and 10-11, depending from claims 2 and 9 respectively, are rejected for failing to alleviate the rejections of claims 2 and 9.

As to claims 6 and 13, the Official Action states that the phrases "the reply control unit is adapted to receive an input control signal, based on which timing information for receiving the external reply from the external device can be determined" and "sending to the reply control unit an input control signal, based on which timing information for receiving the external reply from the external device can be determined" are unclear.

In response, claims 2, 6, 9, and 13 have been amended to overcome the rejection.

Withdrawal of the indefiniteness rejection is solicited.

Other Amendments

Claim 1 has been amended. With reference to the DETAILED DESCRIPTION section, published application paragraph [0022] discusses that Figure 1 shows a block diagram depicting an arrangement in a processor for data packet processing, including a programmable pipeline, through which data packets are transferred in a direction indicated by arrows 110. The pipeline is adapted to perform sequences of instructions on the data packets. Paragraph [0024] discloses that the pipeline includes access points 150. The interface engine is connected to each of the plural access points, via coupling device 160.

As amended, claim 1 requires an interface engine and a programmable pipeline. The structure of the pipeline is now specifically recited. As per claim 1, the pipeline includes a first end and a second end, as well as plural spaced-apart access points therebetween.

Claim 1 has also been amended to recite that the interface engine is adapted to receive a request from any one of the access points of the programmable pipeline, the request being sent upon arrival of one of the data packets at the respective any one access point. See specification page 3, lines 28-29; page 4, line 7; and page 6, lines 10-11.

These features are illustrated at least by Figure 1.

Claim 8 has been similarly amended.

As per the claim, the pipeline is adapted to directionally transfer data packets through from a first end of the pipeline to a second end of the pipeline. The pipeline is also adapted to perform sequences of instructions on the data packets.

The interface engine is connected to each of the plural access points of the pipeline.

The subject matter concerning the pipeline having plural access points was previous recited, e.g., in prior claim 7.

Substantive Rejections: 35 USC 102

The Official Action rejects claims 1-14 under 35 USC 102(b) as being anticipated by DORST, U.S. Publication No. 2004/0098549 A1 (hereinafter, DORST).

The Official Action offers memory controller 1005 as the recited interface engine, which (as per Figure 4), includes circuitry 4010 to external memories 1015A - 1015N. Therefore, the Official Action is reading the "at least one external device" onto these memories.

As to claim 1, the Official Action states that a pipeline is inherent. Although there may be a pipeline, it is not inherent that there is a programmable pipeline, as recited in claim 1. On the contrary, claim 1 as amended recites a programmable pipeline comprising plural access points.

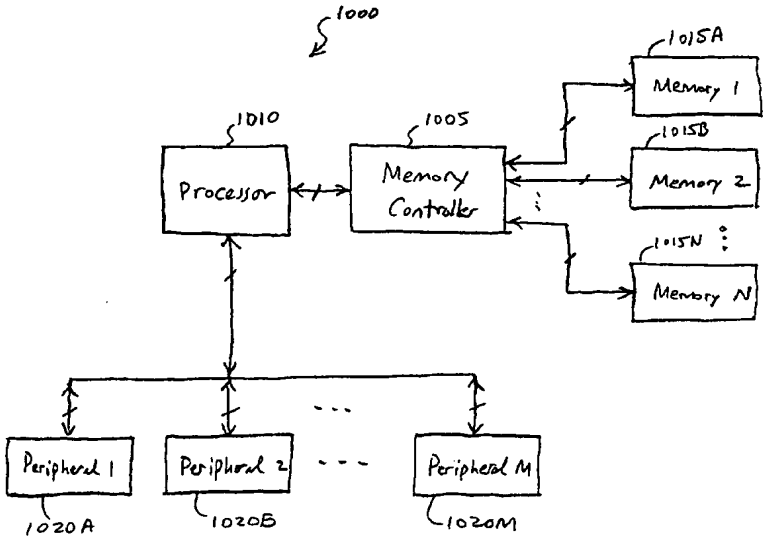



FIG. 1

See DORST Figure 1 above.

DORST discloses a data processing system that includes at least one processor receiving, decoding and executing program instructions (paragraph [0010]). The Official Action states that receiving, decoding, and executing program instructions are steps wherein a pipeline is inherently disclosed.

As to the plural access points, the Official Action relies on DORST paragraph [0031] which discloses that Figure 2 illustrates an embodiment where the memory controller 1005 resides within a processor 1010. The paragraph discloses that the DORST system may have more than one processor 1010 and/or more than one memory controller 1005, as desired. Furthermore, several processors 1010 may share a memory controller 1005.

From this, the Official Action states that the DORST system may comprise plural processors that share a common memory controller.

It is noted that paragraph [0031] of DORST does not mention a pipeline. Indeed, it is noted that DORST does not expressly disclose a pipeline anywhere in the specification or the figures.

The Official Action seems to reason that each processor would necessarily have an access point to the common memory controller, and therefore that there would be plural access points, each processor being an access point. The Official Action seems to further reason that the plural access points inherently define a pipeline to the common memory controller. The Official Action thereby concludes that DORST discloses a programmable pipeline comprising a plurality of access points, as recited by claim 1.

Applicant respectfully disagrees.

As illustrated by Figure 1 of DORST, the processor 1010 may be connected by a line (not numbered) to the memory controller 1005. If there are plural processors, each may be connected to the memory controller by its own line (in a parallel manner). There is nothing in DORST to teach or suggest the pipeline structure as now recited.

Further, although DORST discloses that the memory controller 1005 can service plural processors, there is no

teaching or suggestion that the DORST memory controller is adapted to receive requests from a plurality of access points of a programmable pipeline, the request being sent upon arrival of a data packet at any one of the plurality of access points, as recited in claim 1.

Moreover, if DORST discloses a pipeline as inherent to steps carried out by the processor, i.e. receiving, decoding, and executing instructions, as suggested by the Official Action in paragraph 12, it is not apparent how DORST discloses the processor as an access point to said pipeline, as suggested by the Official Action in paragraph 19. If the processor comprises a pipeline, and the pipeline comprises a plurality of access points as recited in claim 1, it is respectfully submitted that the processor can not be one of a plurality of processors where each processor is an access point.

It is therefore respectfully submitted that DORST does not disclose a programmable pipeline comprising a plurality of access points, wherein at least one interface engine is connected to each of the plural access points, and the at least one interface engine is adapted to receive a request from any one of the access points of the programmable pipeline upon arrival of one of the data packets at the respective access point, as recited in claim 1 as amended.

Accordingly, it is respectfully submitted that claim 1, as amended, is not anticipated by DORST. It is therefore respectfully submitted that claim 1 is patentable.

Reconsideration and withdrawal of the 35 USC 102 rejection of claim 1, and claims depending therefrom, are respectfully requested.

As to independent claim 8, it is respectfully submitted that claim 8 is unanticipated by DORST for the same reasons as those for claim 1 above. In other words, DORST does not disclose a processor comprising a programmable pipeline, the processor being adapted to transfer data packets through the pipeline, and the pipeline comprising a plurality of access points. Therefore, it follows that DORST does not disclose a method step in a processor receiving a request from any one of the access points of a programmable pipeline, the request being received upon arrival of a data packet at the respective any one access point, as recited in claim 8 as amended.

Reconsideration and withdrawal of the rejection of claim 8 and claims depending therefrom is earnestly solicited.

As to claims 7 and 14, the Official Action states that if several processors may share a memory controller, then it is possible that several processors do not share a memory controller. The Official Action states that if a given processor is not able to access all memory controllers, then it is apparent that they cannot send a request to that memory controller either.

The Official Action concludes that because DORST discloses that several processors may share a memory controller, or vice-versa, it is inherent that which is actually the case is adjustable.

Applicant respectfully disagrees. As stated above, DORST does not describe or suggest a programmable pipeline comprising a plurality of access points. It is further submitted that DORST neither describes nor suggests any structure or method wherein a plural element, e.g. plural processors, is adjusted or adjustable.

Accordingly, it is respectfully submitted that DORST does not anticipate a processor whereby the number of access points adapted to send a request to an interface engine adjustable, as recited in claims 7 and 14 as amended.

Reconsideration and withdrawal of the rejection are earnestly solicited.

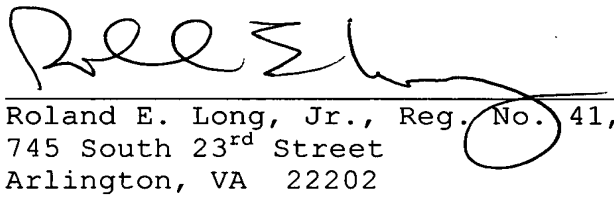
From the foregoing, it will be apparent that applicants have fully responded to the May 3, 2007 Official Action and that the claims as presented are patentable. In view of this, applicants respectfully request reconsideration of the claims, as presented, and their early passage to issue.

In order to expedite the prosecution of this case, it is requested that the Examiner telephone the attorney for applicant at the number set forth below if the Examiner is of the opinion that further discussion of this case would be helpful.

The Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 25-0120 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17.

Respectfully submitted,

YOUNG & THOMPSON



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REL/lk

**Appendix**:

The Appendix includes the following item:

- three replacement sheets for Figures 1-3